

# **BUS SYSTEM AND BUS INTERFACE FOR CONNECTION TO A BUS**

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US2003101311 (A1)

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Abstract not available for JP 2005527877 (T)

Abstract of correspondent: WO 03029998 (A1)

The invention relates to a bus system comprising a first station (202) and a second station (203), (204), coupled by a bus for transferring messages, said bus being designed to operate in accordance with a protocol in which said first station (202) periodically sends messages in a predetermined order to the second station (203), (204), wherein said first station (202) comprises an interruptible processor (206), a memory element (208) comprising a buffer (501, 502), and a bus interface (207), wherein said interruptible processor (206) can be operated so as to generate a plurality of series of message properties, wherein said processor (206) can further be operated so as to issue a first series of message properties from among said plurality of series of message properties to said buffer (501, 503), and upon receipt of an interrupt signal from said bus interface issues a second series of message properties from among said plurality of series of message properties, wherein said buffer (501, 502) has a storage capacity, which is adjustable by the processor (206) and which is matched to store said first series of said message properties and said second series of said message properties; and wherein said bus interface (207) can be operated so as to retrieve said first series of message properties from said buffer, to generate a first series of said messages from said properties, to send said first series of said messages to said second station (203, 204), and to send said interrupt signal to said processor (206).

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